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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,253	03/10/2004	Tony H. Ho	MR1035-1423	2377

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ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,253	HO, TONY H.	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) 9, 17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 9 is objected to because of the following informalities: the limitation "said solder paste" is lacking antecedent basis because solder paste is not disclosed in claim 3 or claim 1. Appropriate correction is required.

Claim 17 is objected to because of the following informalities: the limitation "print circuit board" is lacking antecedent basis because print circuit board is not disclosed in claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 10, 13, 14, 15, 16, 17, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho (U.S. Pre-Grant Publication #2002/0079577).

With respect to **claim 1**, Ho teaches a substrate having a top surface and a bottom surface (Fig. 14, 52), a semiconductor die uplying said top surface (Fig. 14a, 50), a first array comprising a first plurality of solder joints and a second plurality of solder joints (Fig. 14a, 54 and 56), mounted on said die surface and

projecting downwardly, therefrom, said first plurality of solder joints having a higher melting point than said second plurality of solder joints (Col 5 Ln 46), and a second array comprising a third plurality of solder joints (Fig 14a, 58); mounted on said top surface, integral with said first array, therefrom, connecting said die surface and said top surface, and said third plurality of solder joints having a higher melting point than said second plurality of solder joints (Col 5 Ln 48).

With respect to **claim 3**, Ho teaches a printed circuit board underlying a substrate (Fig. 14c, 68), a third ball grid array comprising a fourth plurality of solder joints (Fig. 14c, 64) and a fifth plurality of solder joints (Fig. 14c, 66), mounted on said bottom surface and projecting downwardly, therefrom, said fourth plurality of solder joints having a higher melting point than said fifth plurality of solder joints (Col 5 Ln 55), and a fourth array comprising a sixth plurality of solder joints (Fig. 14c, 70), mounted on said print circuit board, integral with said third array, therefrom, connecting said bottom surface and said print circuit board, and said sixth plurality of solder joints having a higher melting point than said fifth plurality of solder joints (Col 5 Ln 57).

With respect to **claim 10**, Ho teaches a first plurality of solder joints located at four corners of a die surface (Col 8 Ln 23).

With respect to **claim 13**, Ho teaches a fourth plurality of solder joints located at a middle ground plane of a bottom surface of a substrate (Col 8 Ln 29).

With respect to **claim 14**, Ho teaches a structure where a second plurality of solder joints (56, Col 5 Ln 46) and fifth plurality of solder joints (66, Col 5 L 55) have an equal melting point.

With respect to **claim 15**, Ho teaches a structure as described in claim 1 wherein the number of semiconductor dies is more than one (Col 8 Ln 26).

With respect to **claim 16**, Ho teaches that the solder joints implemented on said die surface are heading in correspondence with said solder joints implemented on said top surface (Fig. 14a).

With respect to **claim 17**, Ho teaches that the solder joints implemented on said bottom surface are heading in correspondence with said solder joints on said printed circuit board (Fig. 14c).

With respect to **claim 18**, Ho teaches a semiconductor packaging structure comprising; one semiconductor die (Fig. 1, 10), a printed circuit board underlying said die (Fig. 1, 16), a first array comprising a first plurality of solder joints (Fig. 1, 12) and a second plurality of solder joints (Fig. 1, 14), mounted on said die surface and projecting downwardly (Fig. 1, 10), and a fourth array comprising a sixth plurality of solder joints (Fig. 1, 18), mounted on said printed circuit board, integral with said first array, therefrom, connecting said die surface and said print circuit board (Fig. 1), and said sixth plurality of solder joints having a higher melting point (Col 4 Ln 27) than said second plurality of solder joints (Col 4 Ln 29).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4, 8, 9, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho, in view of Burnette (U.S. Patent #5956606).

With respect to **claim 2**, Ho teaches all of the limitations of claim 1, as well as a first array integral with a second array, at integral process, predetermined the shape of solder joints, said first plurality of solder joints and said third plurality of solder joints were not melted, and said second plurality of solder joints were melted (Fig. 14b). However, Ho does not teach a group of solder paste located between a first array and second array. Burnette teaches a solder paste located between two solder joints (Fig. 11, 316 and Col 5 Ln 27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ho and Burnette to use solder paste in connecting the first and second arrays in order to enhance the electrical and mechanical reliability of the connection.

With respect to **claim 4**, Ho teaches all of the limitations of claim 1, as well as a third array and a fourth array; said third array integral with said fourth array, at integral process (Fig. 14c and Fig. 14d), predetermined the shape of solder

joints, said fourth plurality of solder joints and said sixth plurality of solder joints were not melted, and said fifth plurality of solder joints were melted (Fig. 14d). However, Ho does not teach a group of solder paste located between said third array and said forth array. Burnette teaches a solder paste located between two solder joints (Fig. 11, 316 and Col 5 Ln 27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ho and Burnette to use solder paste in connecting the third and forth arrays in order to enhance the electrical and mechanical reliability of the connection.

With respect to **claim 8**, Ho and Burnette teach all of the limitations of claim 2, and also teach that when said semiconductor package has been assembled, said first plurality of solder joints and said sixth plurality of solder joints were not melted; and said second plurality of solder joints and said solder paste were melted (Ho, Fig. 14b).

With respect to **claim 9**, Ho and Burnette teach all of the limitations of claim 3, and also teach that when said semiconductor package has been assembled, said fourth plurality of solder joints and said sixth plurality of solder joints were not melted; and said fifth plurality of solder joints and said solder paste were melted (Ho, Fig. 14d).

With respect to **claim 19**, Ho teaches all of the limitations of claim 18, and also teaches a first array integral with said fourth array, at integral process, predetermined the shape of solder joints, said first plurality of solder joints and

said sixth plurality of solder joints were not melted, and said second plurality of solder joints were melted (Fig. 1 after reflow procedure). However, Ho does not teach a solder paste located between said first array and said fourth array. Burnette teaches a solder paste located between two solder joints (Fig. 11, 316 and Col 5 Ln 27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ho and Burnette to use solder paste in connecting the first and forth arrays in order to enhance the electrical and mechanical reliability of the connection.

Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho, in view of Sakurai et al (U.S. Patent #6455785), hereafter known as Sakurai.

With respect to **claim 5**, Ho teaches all of the limitations of claim 1, but does not teach a solder joint comprising a flat surface at its front edge. Sakurai teaches a bump connection with a flat upper surface (Fig. 7, 34 and Col 5 Ln 22). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder joints comprising a flat surface at its front edge in order to facilitate easier stacking of the joints.

With respect to **claim 6**, Ho and Sakurai teach all of the limitations of claim 5, but Ho does not teach that said flat surface implemented on said die surface is 3% to 70% smaller than said corresponding flat surface implemented on said top surface. Sakurai teaches a bump with a small flat surface (Fig. 23,

58) connected on top of a bump with a larger flat surface than the top bump (Fig. 23, 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ho and Sakurai to use solder joints comprising a flat surface where the solder joints on the die surface are 3% to 70% smaller than the flat surfaces on the top surface in order to increase the structural integrity of the connection.

With respect to **claim 7**, Ho and Sakurai teach all of the limitations of claim 5, but Ho does not teach that said flat surface implemented on said bottom surface is 3% to 70% smaller than said corresponding flat surface implemented on said printed circuit board. Sakurai teaches a bump with a small flat surface (Fig. 23, 58) connected on top of a bump with a larger flat surface than the top bump (Fig. 23, 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ho and Sakurai to use solder joints comprising a flat surface where the solder joints on the bottom surface are 3% to 70% smaller than the flat surfaces on the printed circuit board in order to increase the structural integrity of the connection.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ho, in view of Kumazawa et al (U.S. Patent #5569960).

With respect to **claim 11**, Ho teaches all of the limitations of claim 1, but does not teach a first plurality of solder joints located at a middle ground plane of said die surface. Kumazawa teaches a middle plane comprising solder joints of

a different melting point to connect a die and a substrate (Fig. 7, 8 and Col 10 Ln 47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ho and Kumazawa to have said first plurality of solder joints in the middle ground plane of said die surface in order to enhance the structural integrity of the connection.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ho, in view of Kiowa et al (U.S. Patent #5907187), hereafter known as Kiowa.

With respect to **claim 12**, Ho teaches all of the limitations of claim 3, but does not teach a forth plurality of solder joints located at four corners of said bottom surface. Kiowa teaches a plurality of high melting solder joints at the four corners of a bottom substrate (Fig. 1, 6b and Col 14 Ln 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ho and Kiowa by placing a forth plurality of solder joints at the four corners of a bottom surface in order to enhance the structural integrity of the connection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Everyday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on M-F. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

bps